

Amendments to the Claims

1. *(Currently Amended)* An electronic circuit, comprising an asynchronously operated FIFO pipe-line ~~(10a-d)~~, the FIFO pipeline ~~(10a-d)~~ comprising a plurality of handshake chains functionally in parallel, for passing successive data items each by passing a handshake through a selected one of the handshake chains, the selected one of the handshake chains being selected dependent on a value of the data item, the FIFO pipeline ~~(10a-d)~~ comprising successive pipe-line stages, each pipe-line stage comprising respective handshake stages ~~(12, 16)~~ of each of the plurality of handshake chains, and a coordination circuit ~~(15)~~ arranged to prevent handshakes in mutually different ones of handshake chains from overtaking one another.

2. *(Currently Amended)* An electronic circuit according to claim 1, comprising

- a data source circuit ~~(1)~~ with a data output ~~(D)~~ for signalling the value of the data item;
- an interface circuit coupled between the source circuit ~~(1)~~ and the FIFO pipe-line ~~(10a-d)~~, the interface circuit having a plurality of output handshake interfaces ~~((REQ1_i, ACK1_i), (REQ0_i, ACK0_i))~~ coupled to respective ones of the handshake chains, and an interface selection input coupled to the data output ~~(D)~~ for selecting, under control of the value, one of the output handshake interfaces ~~((REQ1_i, ACK1_i), (REQ0_i, ACK0_i))~~ on which to start a handshake transaction for the value.

3. *(Currently Amended)* An electronic circuit according to claim 1, comprising

- a data sink circuit ~~(2)~~ with a data input ~~(D)~~ for receiving the value of the data item;
- an interface circuit coupled between the FIFO pipe-line ~~(10a-d)~~ and the sink circuit ~~(2)~~, the interface circuit having a plurality of input handshake interfaces ~~((REQ1_o, ACK1_o), (REQ0_o, ACK0_o))~~ coupled to respective ones of the handshake chains, the interface circuit being arranged to apply a data signal to the data input ~~(D)~~ upon receiving a respective handshake on any one of the input

handshake interfaces ~~((REQ1_o, ACK1_o), (REQ0_o, ACK0_o))~~, the interface circuit controlling a value of the data signal dependent on the input handshake interface ~~((REQ1_o, ACK1_o), (REQ0_o, ACK0_o))~~ from which the respective handshake was received.

4. *(Original)* An electronic circuit according to claim 1, wherein at least one of the handshake stages is not coupled to a timing input of any latch with a data input for storing the values of the data items.

5. *(Currently Amended)* An electronic circuit according to Claim 1, wherein the coordination circuit ~~(15)~~ of a particular pipe-line stage ~~(10a-d)~~ is arranged to delay acknowledgement of incoming requests on any of the handshake stages ~~(12, 16)~~ of the particular pipe-line stage ~~(10a-d)~~ while an outgoing handshake request is pending on any of the handshake stages ~~(12, 16)~~.

6. *(Currently Amended)* An electronic circuit according to Claim 1, wherein each pipe-line stage ~~(10a-d)~~ comprises

- a plurality of input handshake interfaces ~~((REQ1_i, ACK1_i), (REQ0_i, ACK0_i))~~ in parallel, each for handling incoming requests from a respective one of the handshake chains;
- a plurality of output handshake interfaces ~~((REQ1_o, ACK1_o), (REQ0_o, ACK0_o))~~ in parallel, each for generating outgoing requests in a respective one of the handshake chains
- a memory circuit ~~(20, 22)~~ coupled to the input handshake interfaces ~~((REQ1_i, ACK1_i), (REQ0_i, ACK0_i))~~ and the output handshake interfaces ~~((REQ1_o, ACK1_o), (REQ0_o, ACK0_o))~~, for representing whether completion of transmission of a request from any of the input handshake interfaces ~~((REQ1_i, ACK1_i), (REQ0_i, ACK0_i))~~ to any of the output handshake interfaces ~~((REQ1_o, ACK1_o), (REQ0_o, ACK0_o))~~ is pending;
- the coordination circuit ~~(24)~~ having an input coupled to the memory circuit ~~(20, 22)~~ and an output coupled to the input handshake interfaces ~~((REQ1_i, ACK1_i), (REQ0_i, ACK0_i))~~ to prevent acknowledgement of incoming handshakes when the memory circuit ~~(20, 22)~~ represents that an outgoing handshake is pending.

7. *(Currently Amended)* An electronic circuit according to claim 1, wherein four phase signalling is used in the handshake chains, each handshake stage comprising

- an input combination of a request line and an acknowledge line ~~((REQ1_i, ACK1_i), (REQ0_i, ACK0_i))~~, for handling incoming requests from a respective one of the handshake chains;
- an output combination of a request line and an acknowledge line ~~((REQ1_o, ACK1_o), (REQ0_o, ACK0_o))~~, for handling outgoing requests for the respective one of the handshake chains;
- a logic gate ~~(26, 28)~~ having a first logic input and a logic output coupled the request line ~~((REQ1_i, REQ0_i))~~ and the acknowledge line ~~(ACK1_i, ACK0_i)~~ of the input combination respectively;
- a set-reset latch ~~(20, 22)~~ with a set input coupled to the output of the logic gate ~~(26, 28)~~, a data output coupled to the request line of the output combination ~~(REQ1_o, REQ0_o)~~, a reset input coupled to the acknowledge line ~~(ACK1_o, ACK0_o)~~ of the output combination, and a not-data output coupled to the coordination circuit ~~(24)~~;
- wherein the coordination circuit ~~(24)~~ is arranged to disable response of the logic gates ~~(26, 28)~~ of all handshake stages in the pipeline stage while the not-data output of any one of the set-reset latches ~~(20, 22)~~ of the pipeline stage indicates a set state.

8. *(Currently Amended)* An electronic circuit according to claim 7, wherein mutually opposite active levels are used for request and acknowledgement signals on the request lines ~~(REQ1_i, REQ1_o, REQ0_i, REQ0_o)~~ and acknowledge lines ~~(ACK1_i, ACK1_o, ACK0_i, ACK0_o)~~ respectively.

9. (Original) An electronic circuit according to claim 1, wherein the plurality of handshake chains consists of two handshake chains for passing binary values of data items.